ABSTRACT

A nonvolatile memory array is arranged as a plurality of rows and columns of memory cell transistors. The sources of the memory cell transistors in each row of the array are electrically coupled together. The control gates of the memory cell transistors associated with a row in the array are coupled to a wordline associated with that row. The drains of the memory cell transistors in a column of the array are coupled to a bitline associated with that column. A source transistor is associated with each row and has its source coupled to a common source line, its drain coupled to the sources of all memory cell transistors in that row, and a gate coupled to the wordline. An array of split-gate nonvolatile memory cells is also disclosed.